

FIG. 1

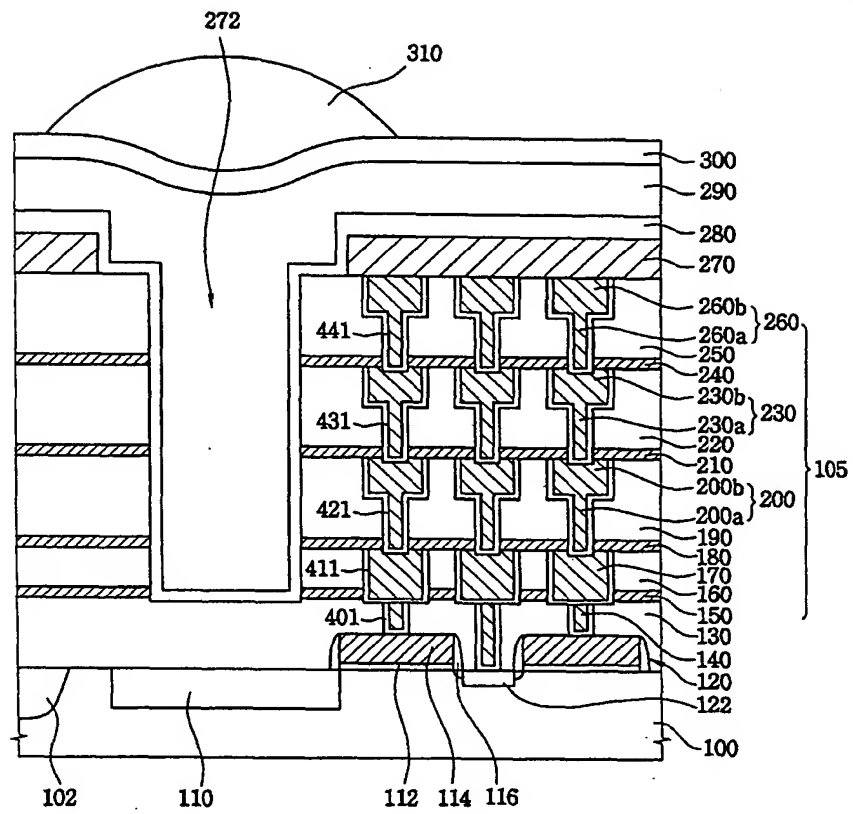


FIG. 2A

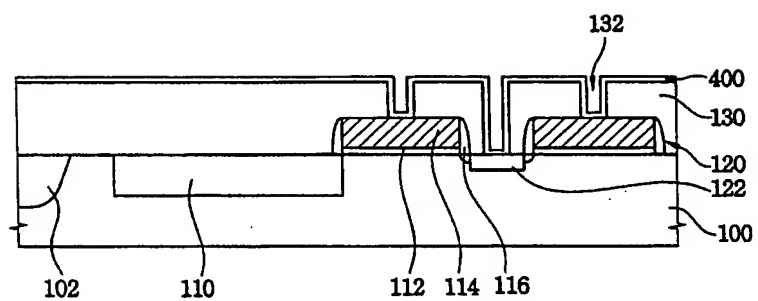


FIG. 2B

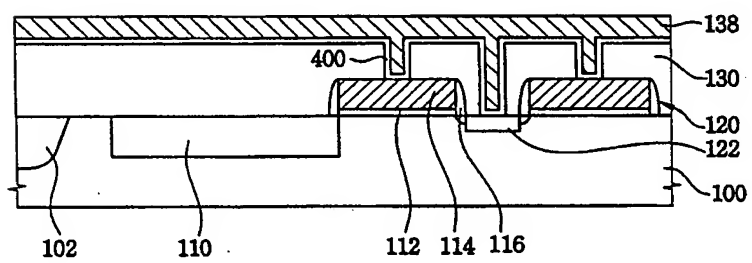


FIG. 2C

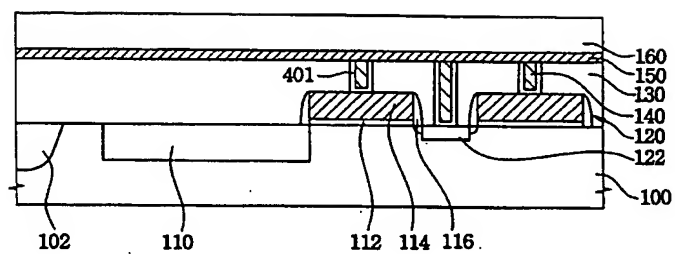


FIG. 2D

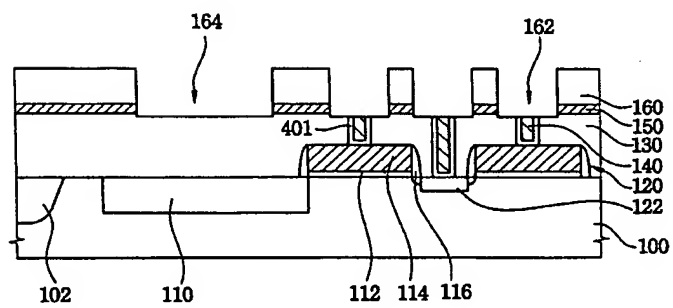


FIG. 2E

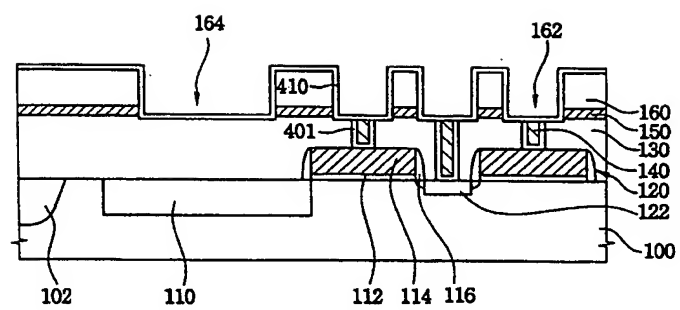


FIG. 2F

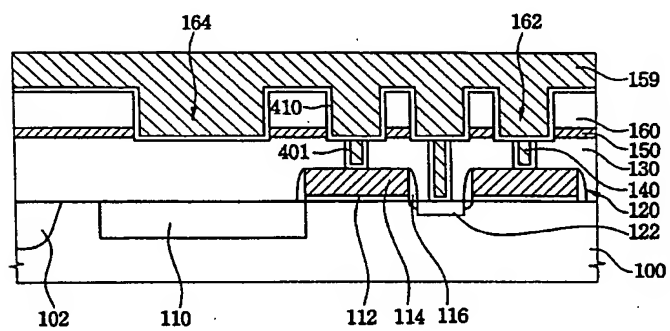


FIG. 2G

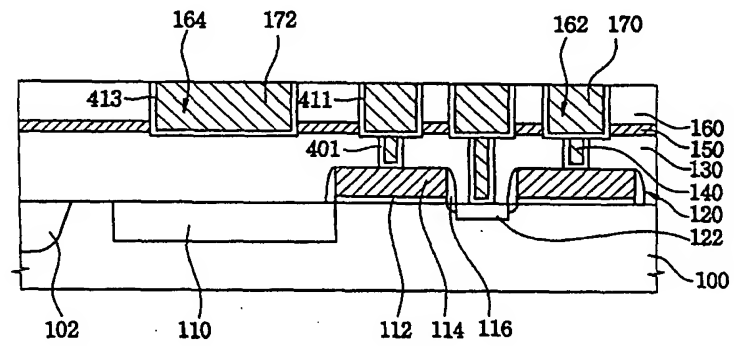


FIG. 2H

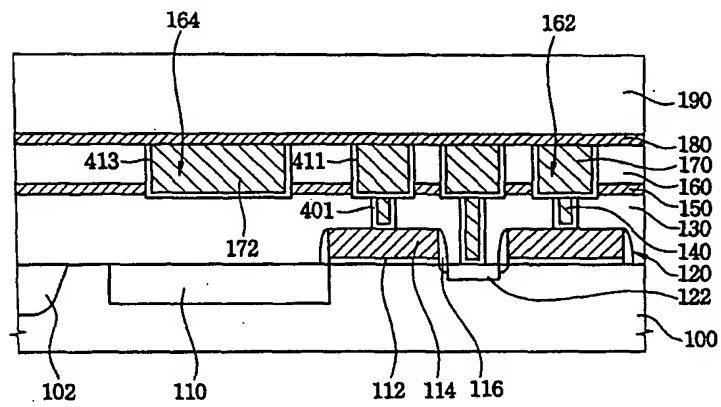


FIG. 2I

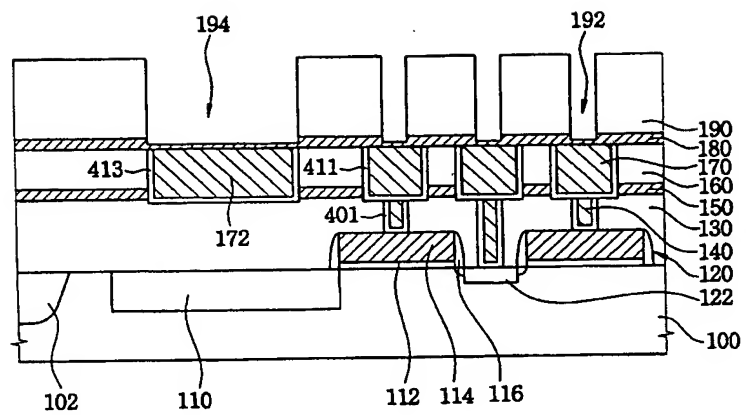


FIG. 2J

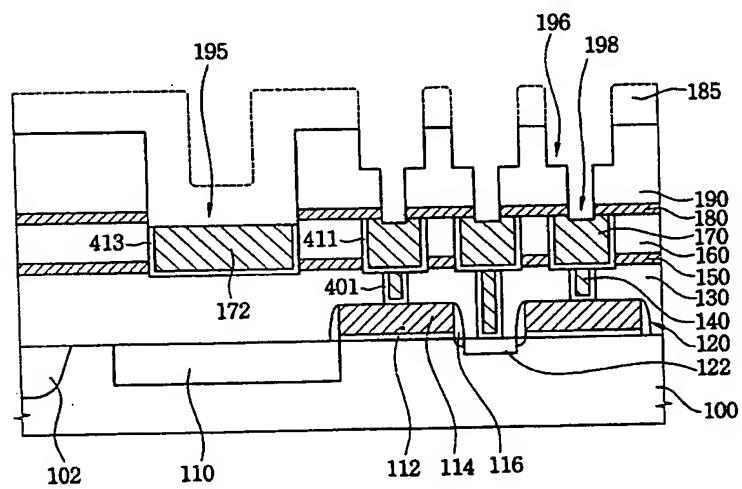


FIG. 2K

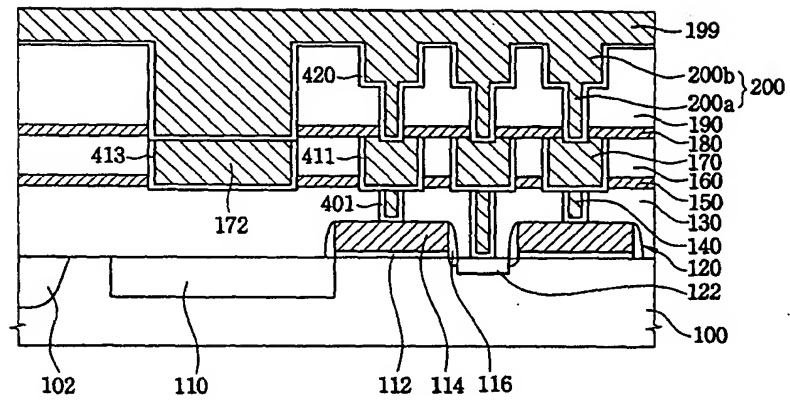


FIG. 2L

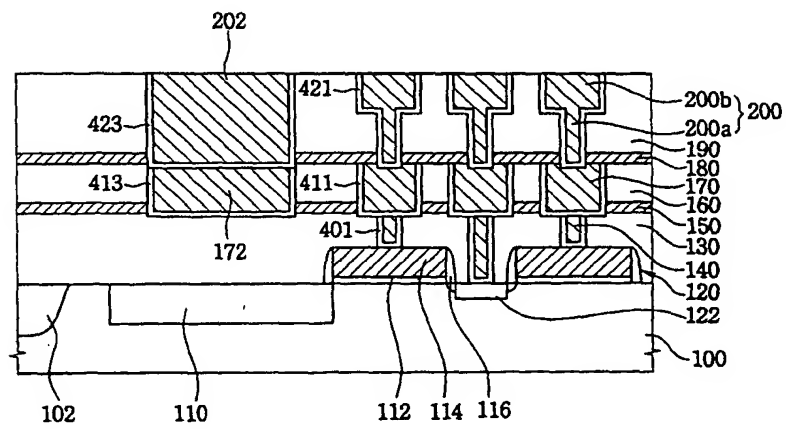


FIG. 2M

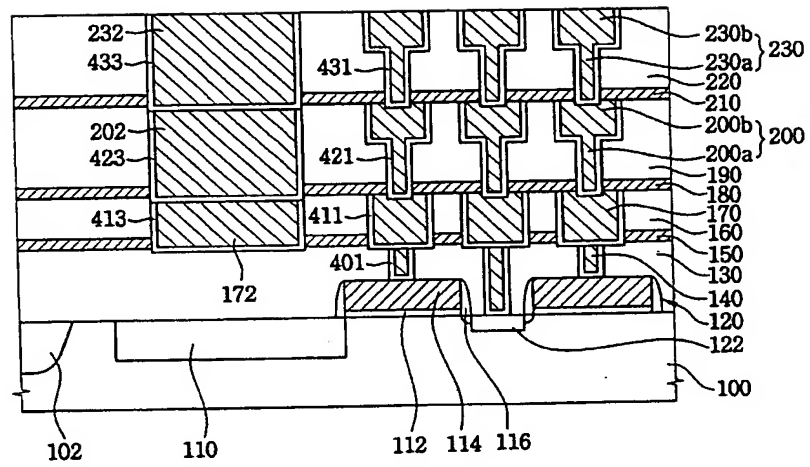




FIG. 2N

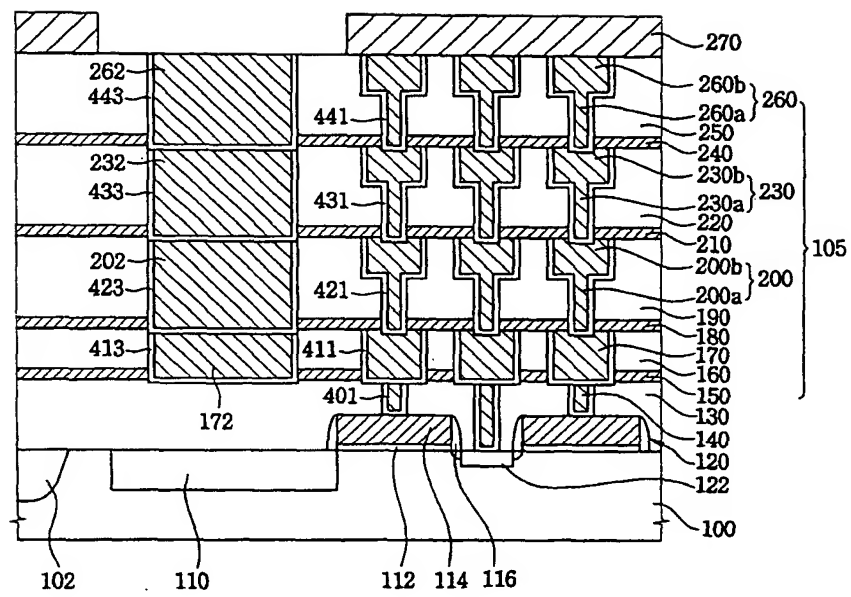


FIG. 20

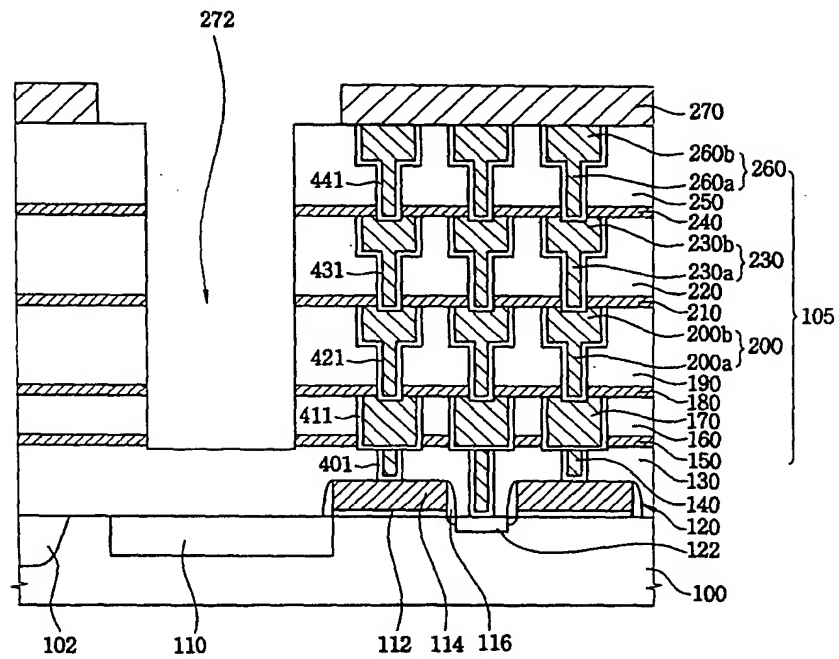


FIG. 2P

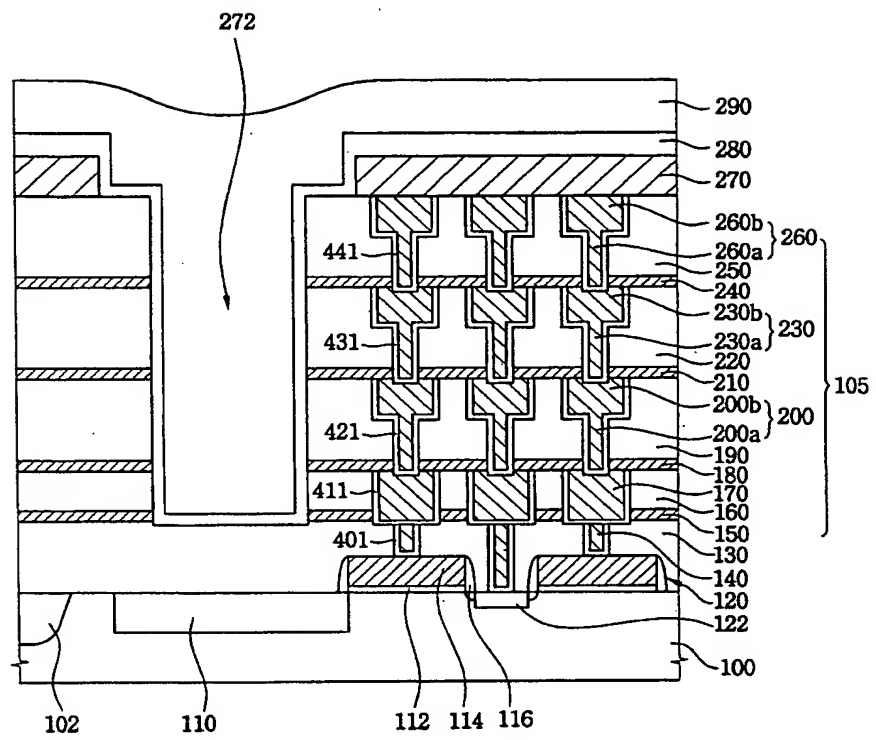


FIG. 2Q

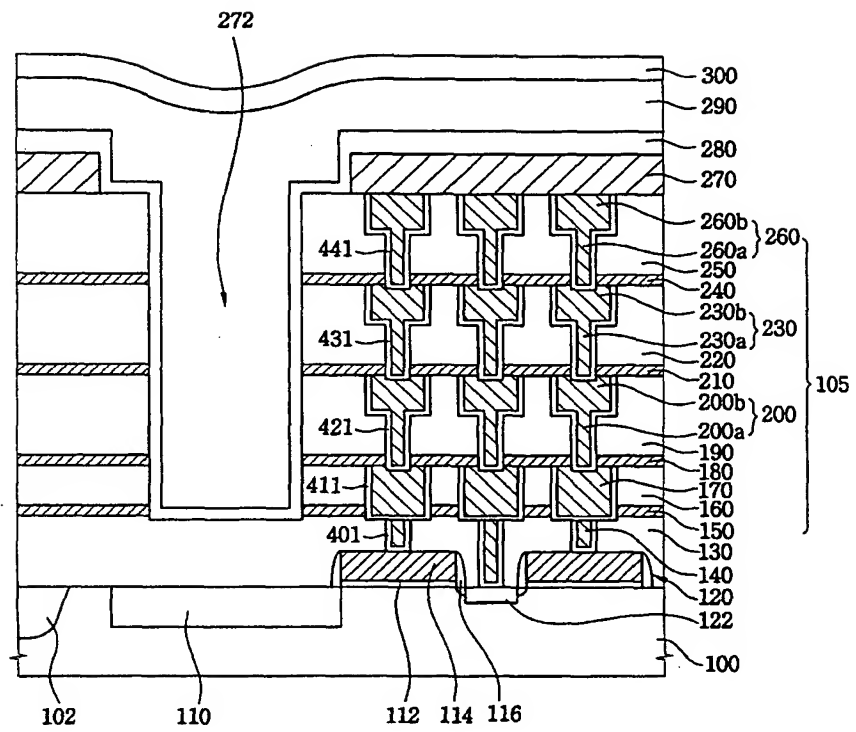


FIG. 2R

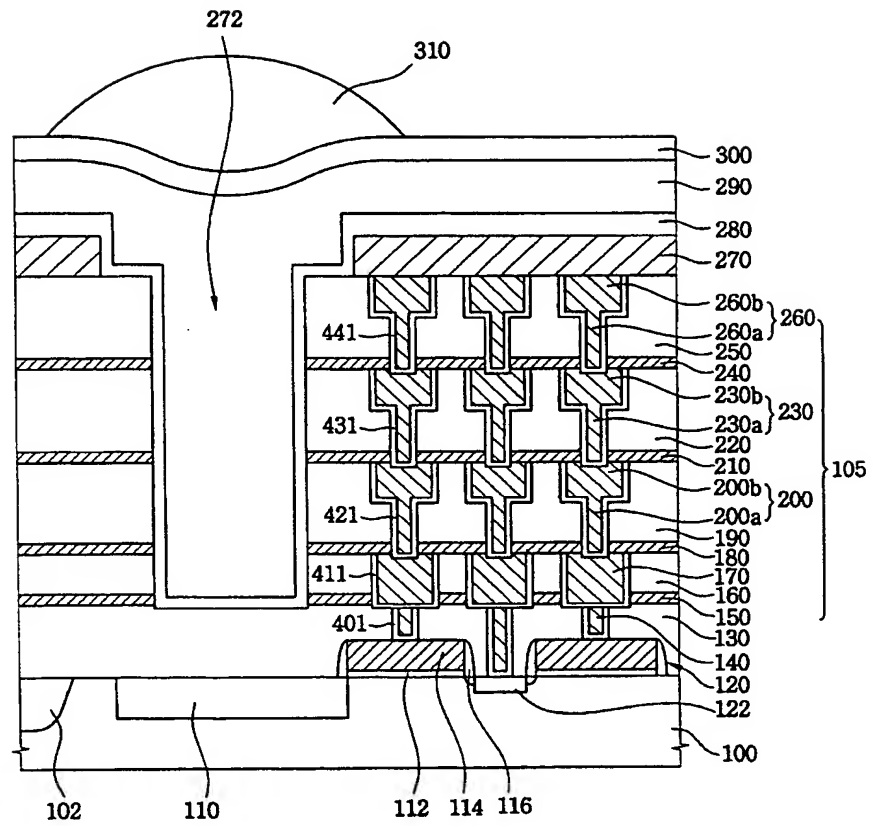
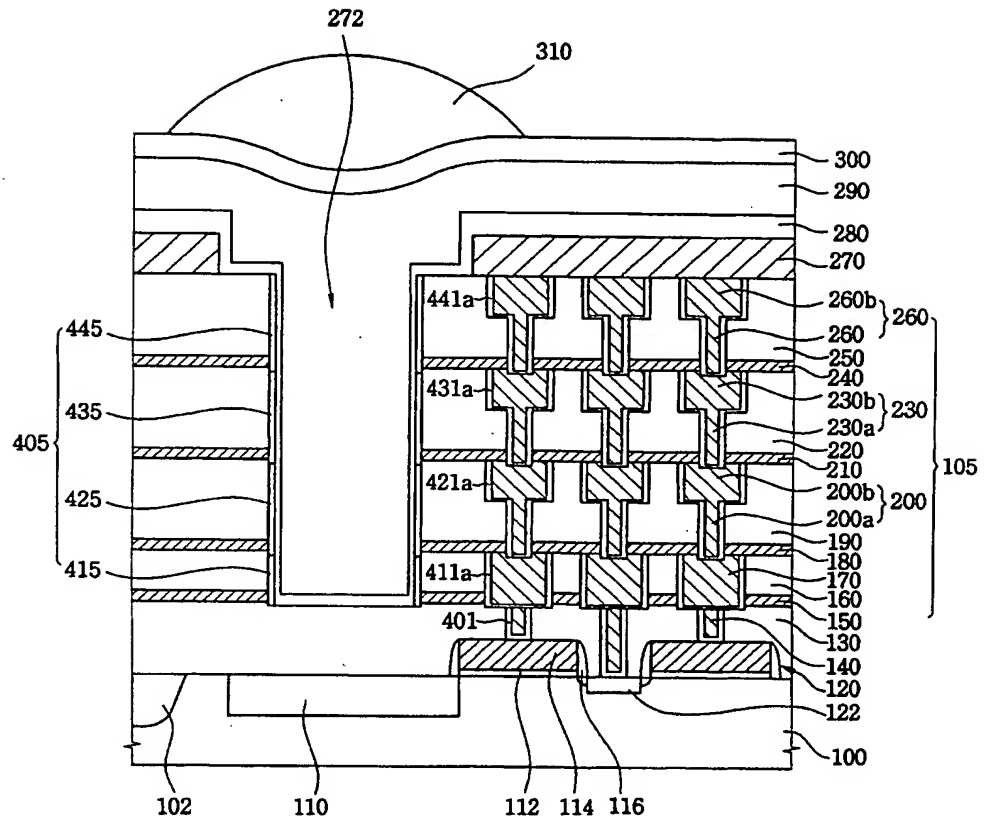


FIG. 3





This cross-sectional view shows a semiconductor device with a substrate 100. A base layer 102 is formed on the substrate. A series of layers are deposited on top: 110, 122, 120, 140, 130, 150, 160, 170, 180, and 190. The 190 layer contains openings 301 and 302. A layer 190' is located between the 190 layer and the 180 layer. A layer 413a is formed on the 190 layer, with openings 411a and 413a. A layer 172 is formed on the 413a layer. A layer 401 is formed on the 172 layer, with openings 112, 114, and 116. A layer 110 is formed on the 401 layer, with openings 102 and 110. A layer 102 is formed on the 110 layer, with openings 102 and 110.

[illegible]



FIG. 4E

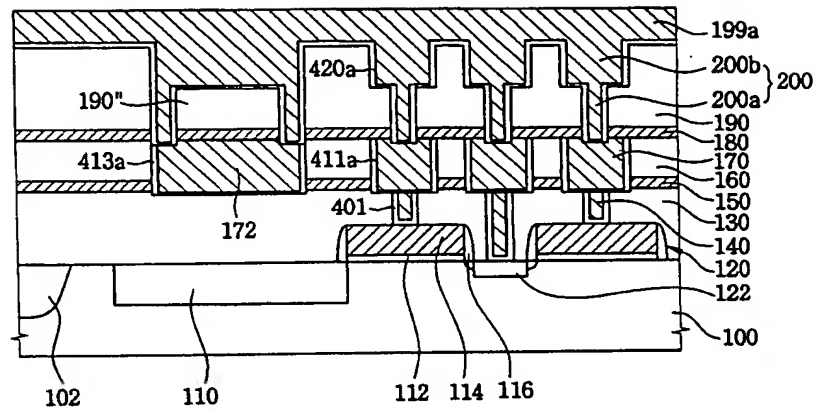


FIG. 4F

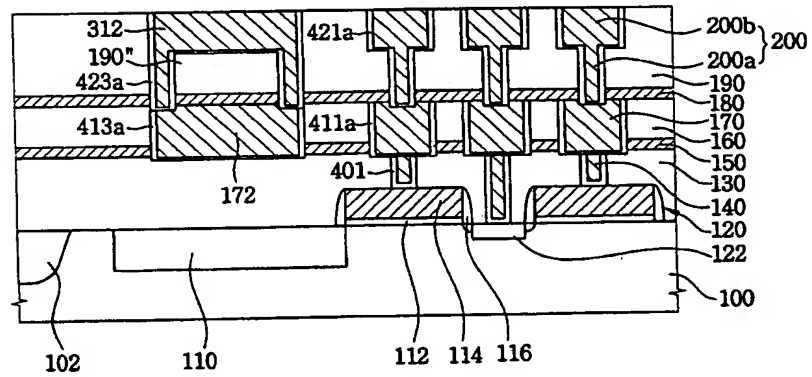


FIG. 4G

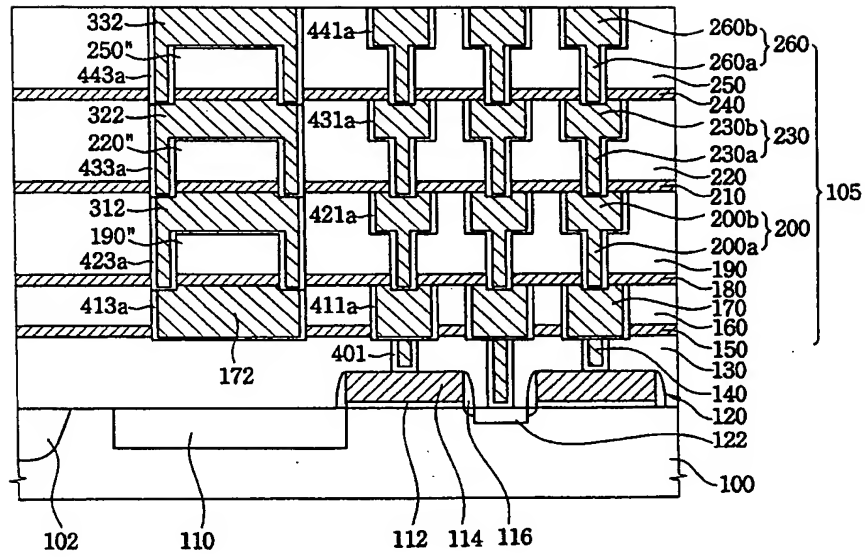


FIG. 4H

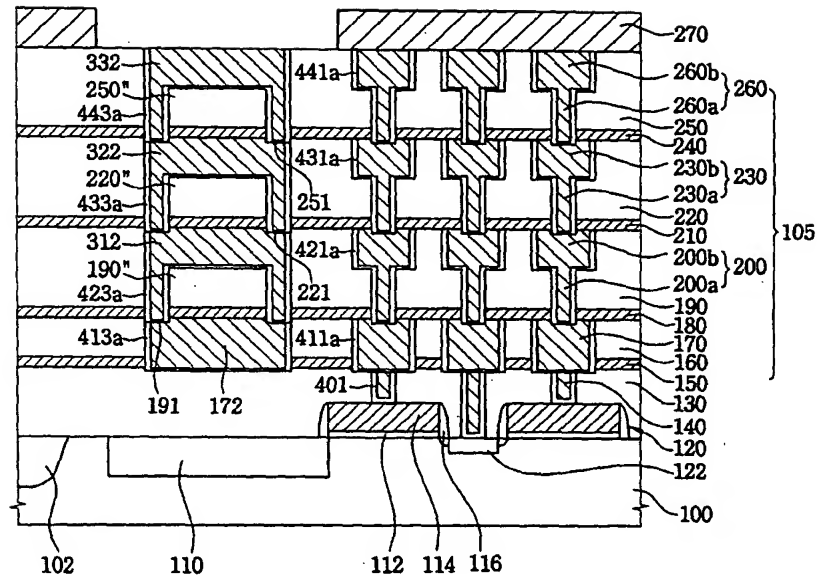


FIG. 4I

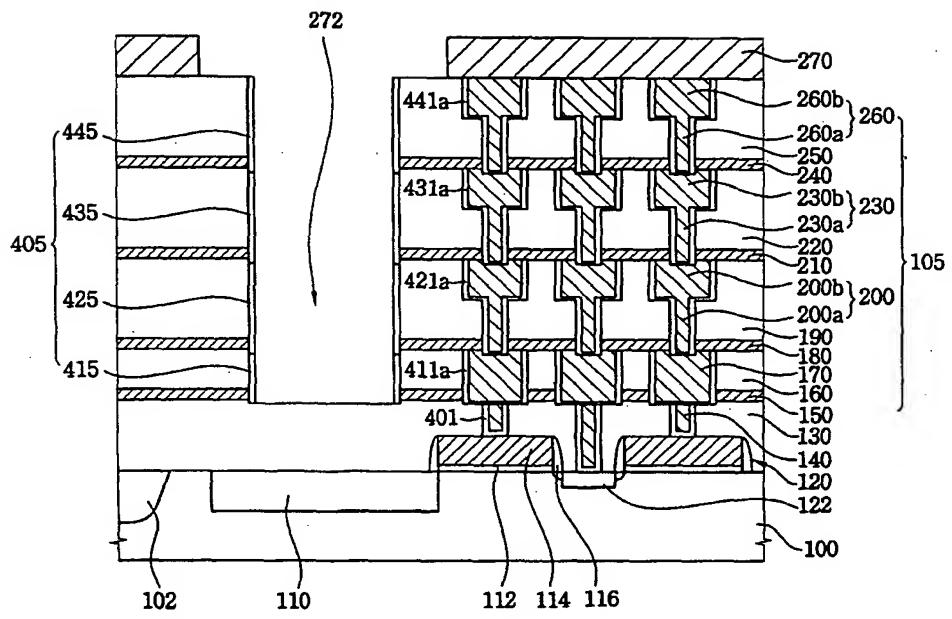


FIG. 4J

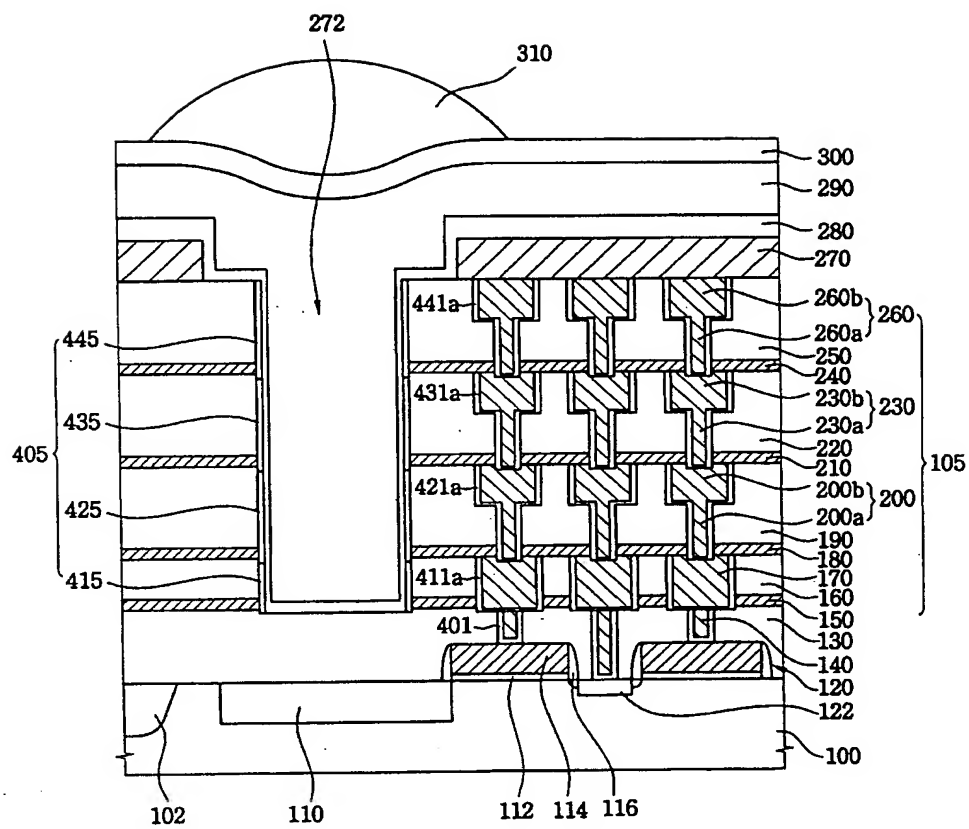


FIG. 5

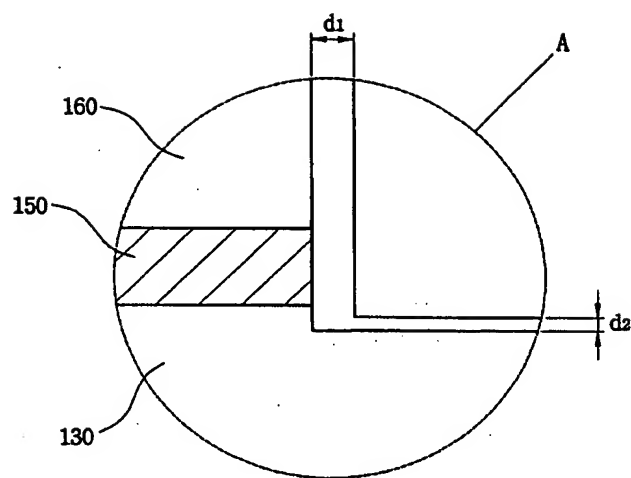


FIG. 6A

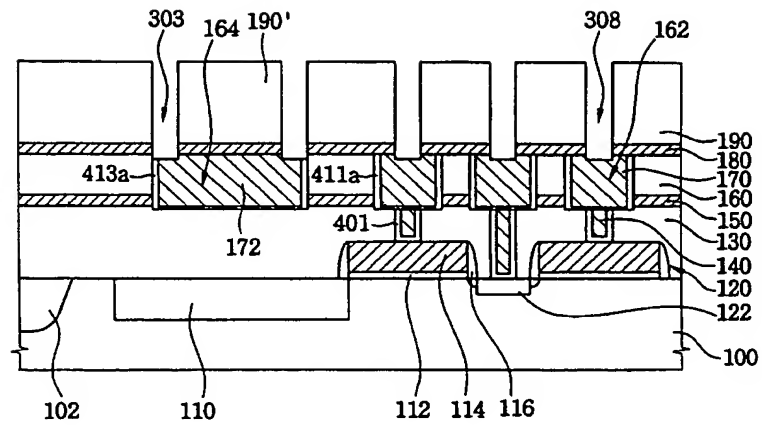


FIG. 6B

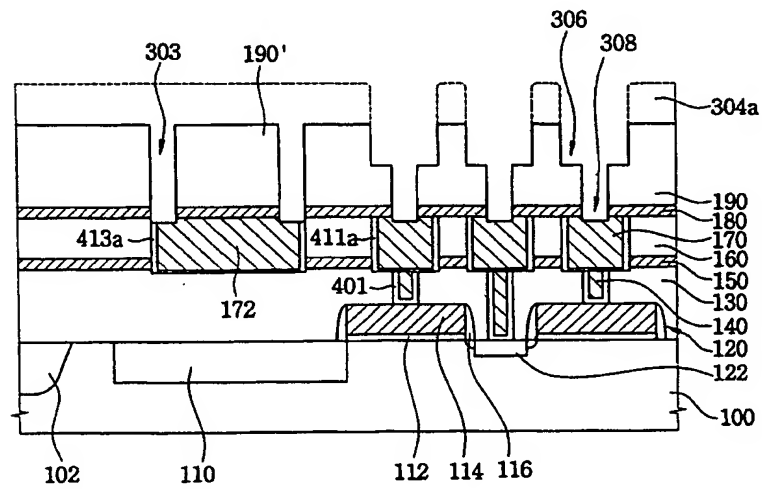


FIG. 6C

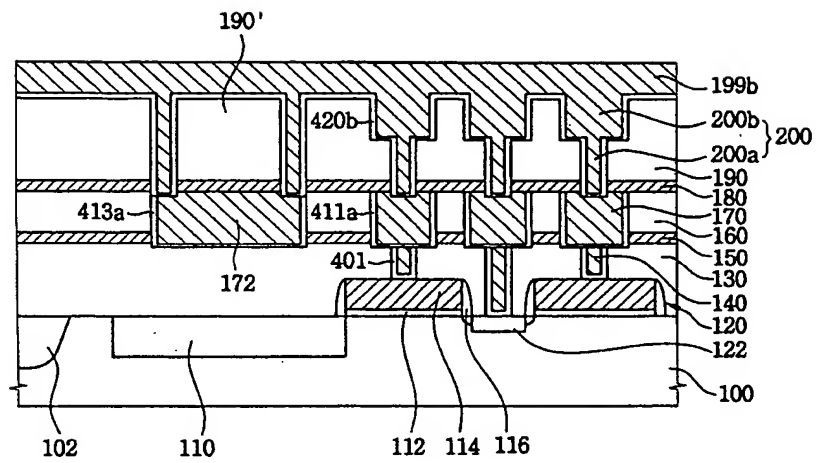


FIG. 6D

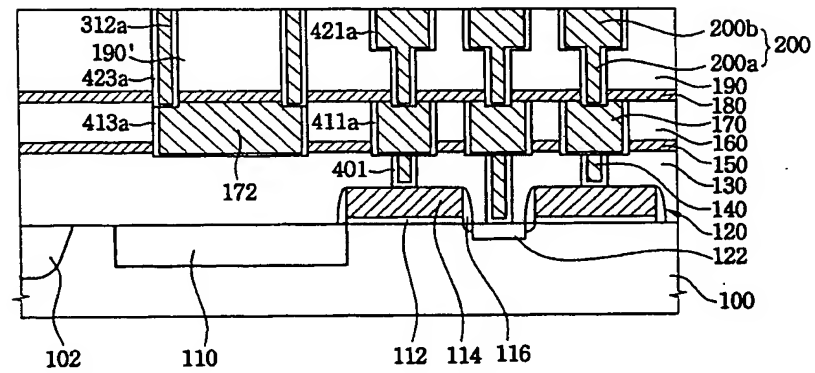




FIG. 6E

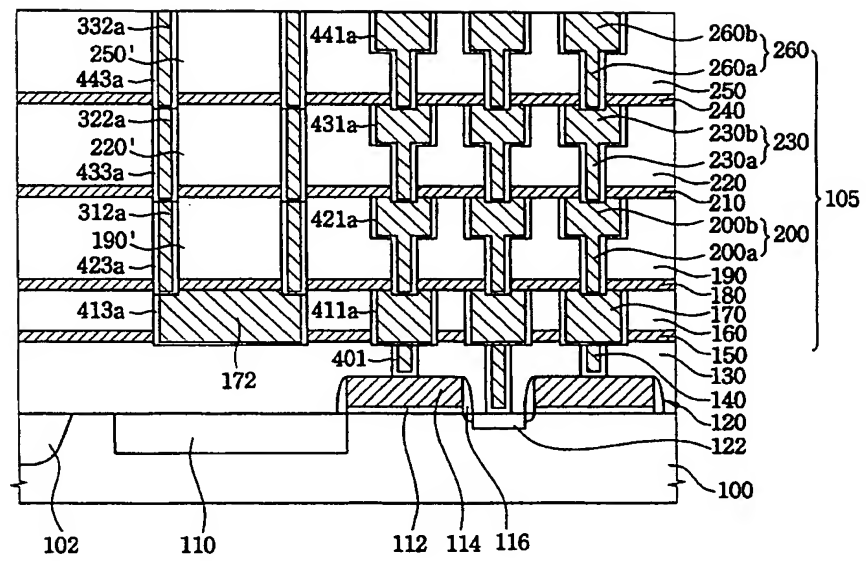


FIG. 6F

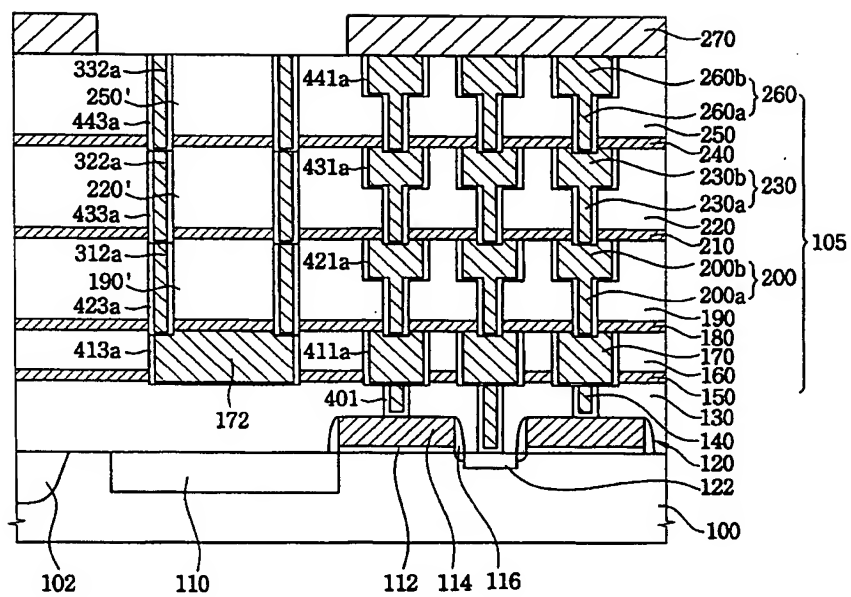


FIG. 6G

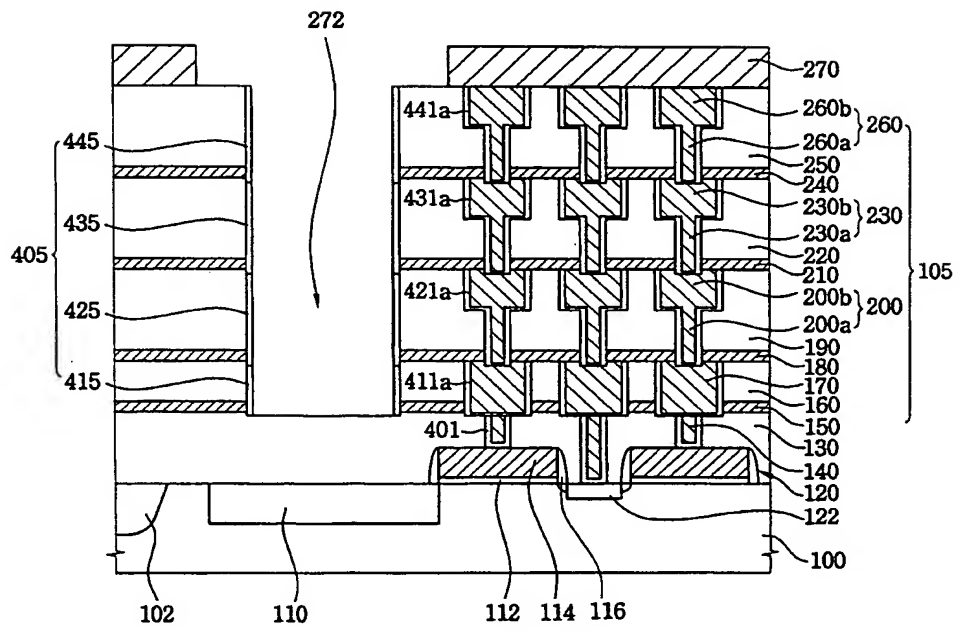


FIG. 6H

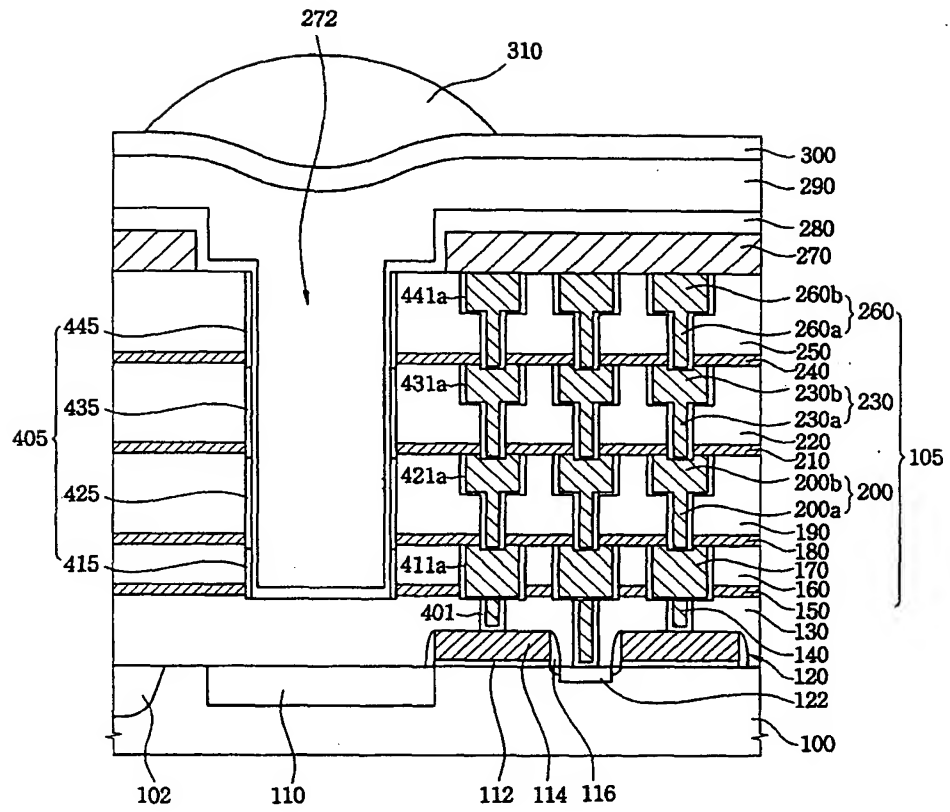


FIG. 7A

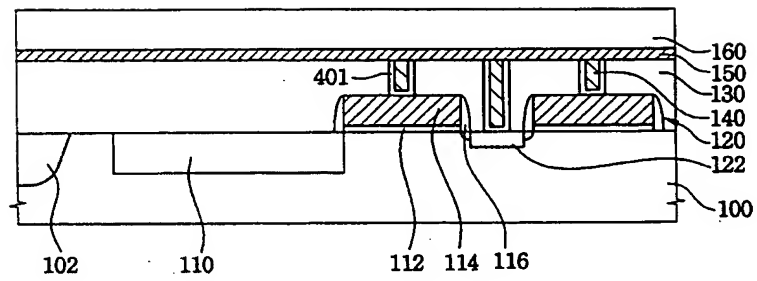


FIG. 7B

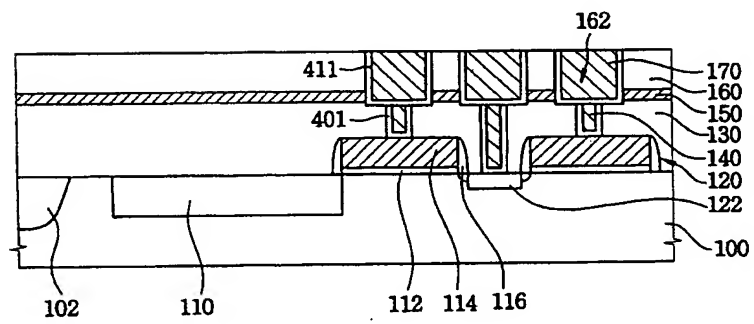


FIG. 7C

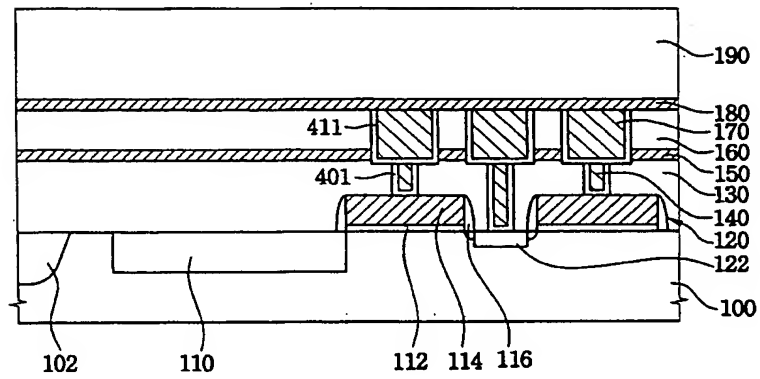


FIG. 7D

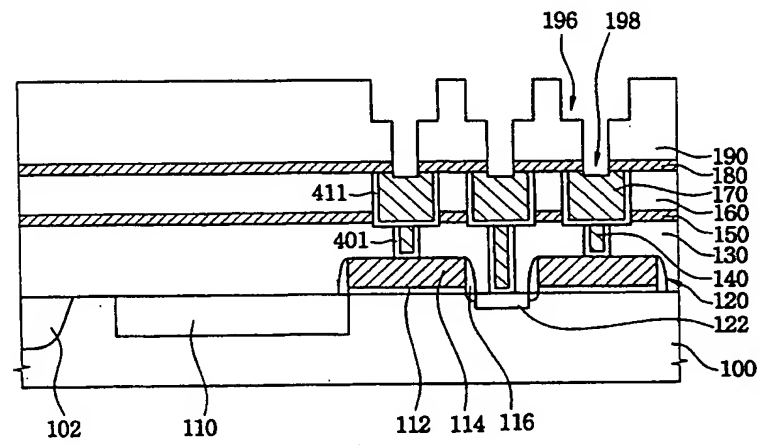


FIG. 7E

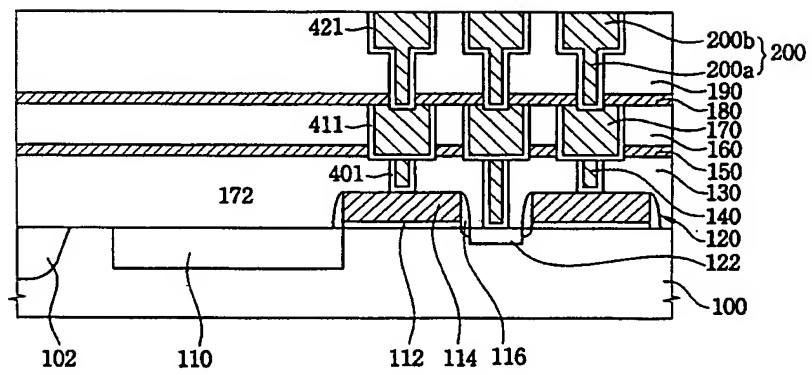


FIG. 7F

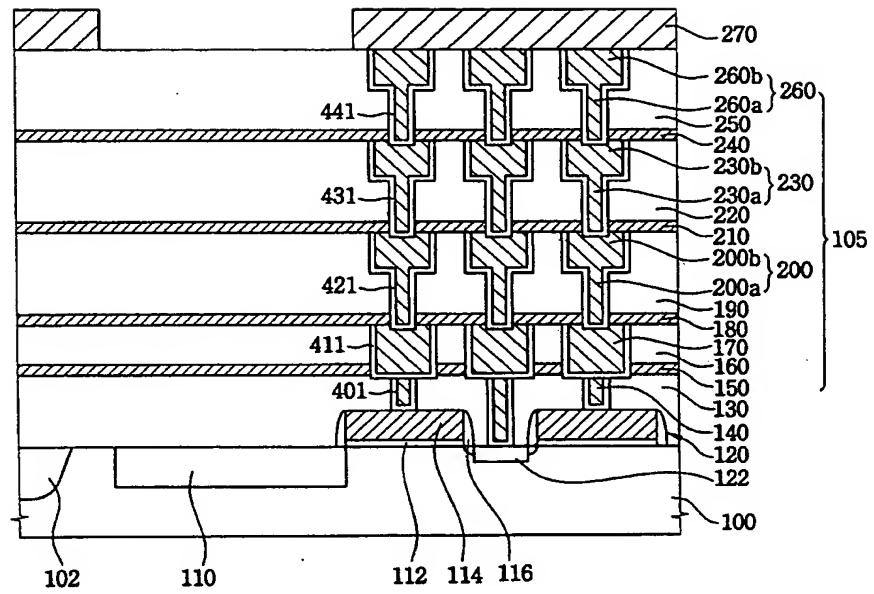




FIG. 7G

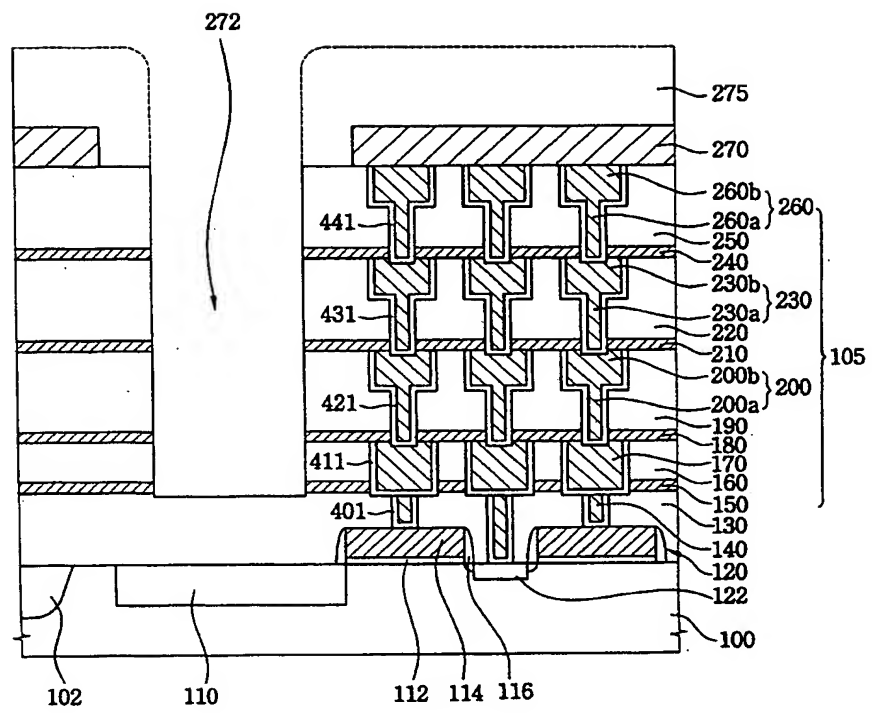


FIG. 7H

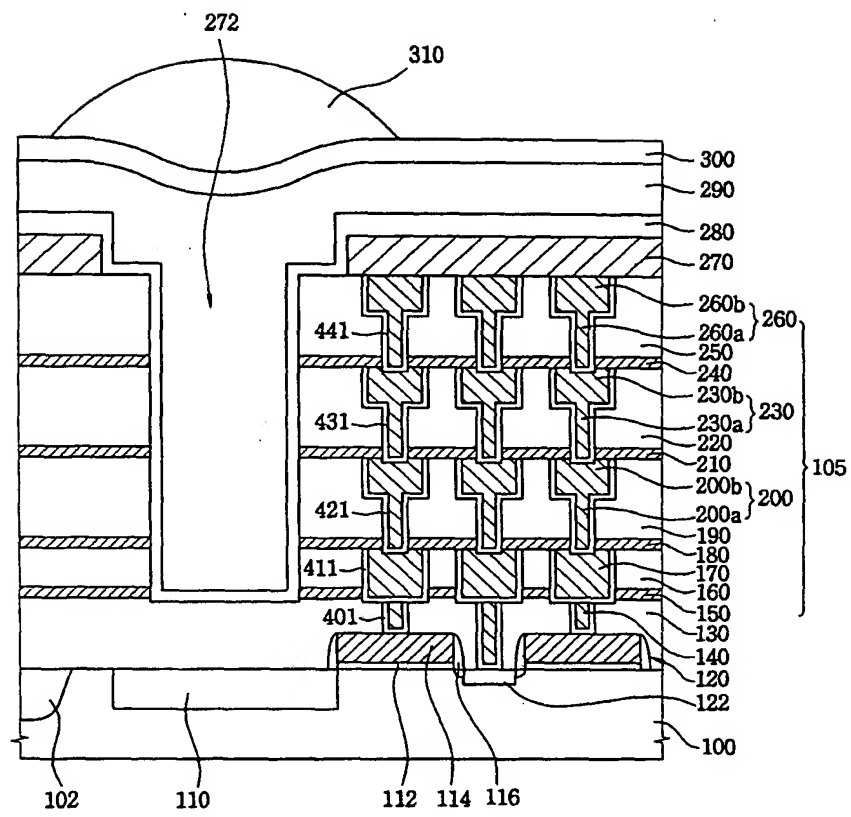


FIG. 8

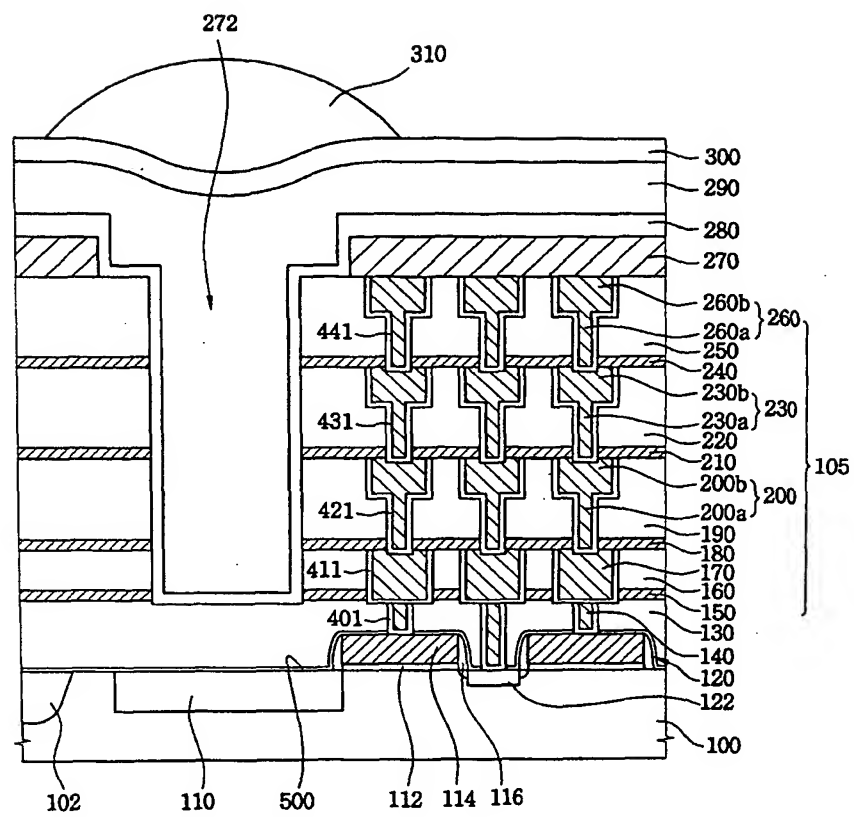


FIG. 9

